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Sensor Modules for Wireless Distributed Sensor Networks

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Purpose and Overall Concept

A national security need as well as environmental monitoring need exists for networks of sensors. The advantages of a network of sensors over a single sensor are improved range, sensitivity, directionality, and data readability. Depending upon the particular application, sensors can be acoustic, chemical, biological, thermal or inertial. A major desire in these sensor networks is to have the individual sensor and associated electronics small and low enough in power that the battery can also be small and of long life. Smaller, low power sensor nodes can allow more nodes per network. A typical network for security applications is depicted in **Figure 1**. Here a number of sensor nodes are deployed around a central hub node in a star configuration. In this scenario the hubs communicate with each other and ultimately relay information to a satellite. Future networks might follow this scenario or some other network architecture such as a hopping network where individual nodes communicate directly with each other.

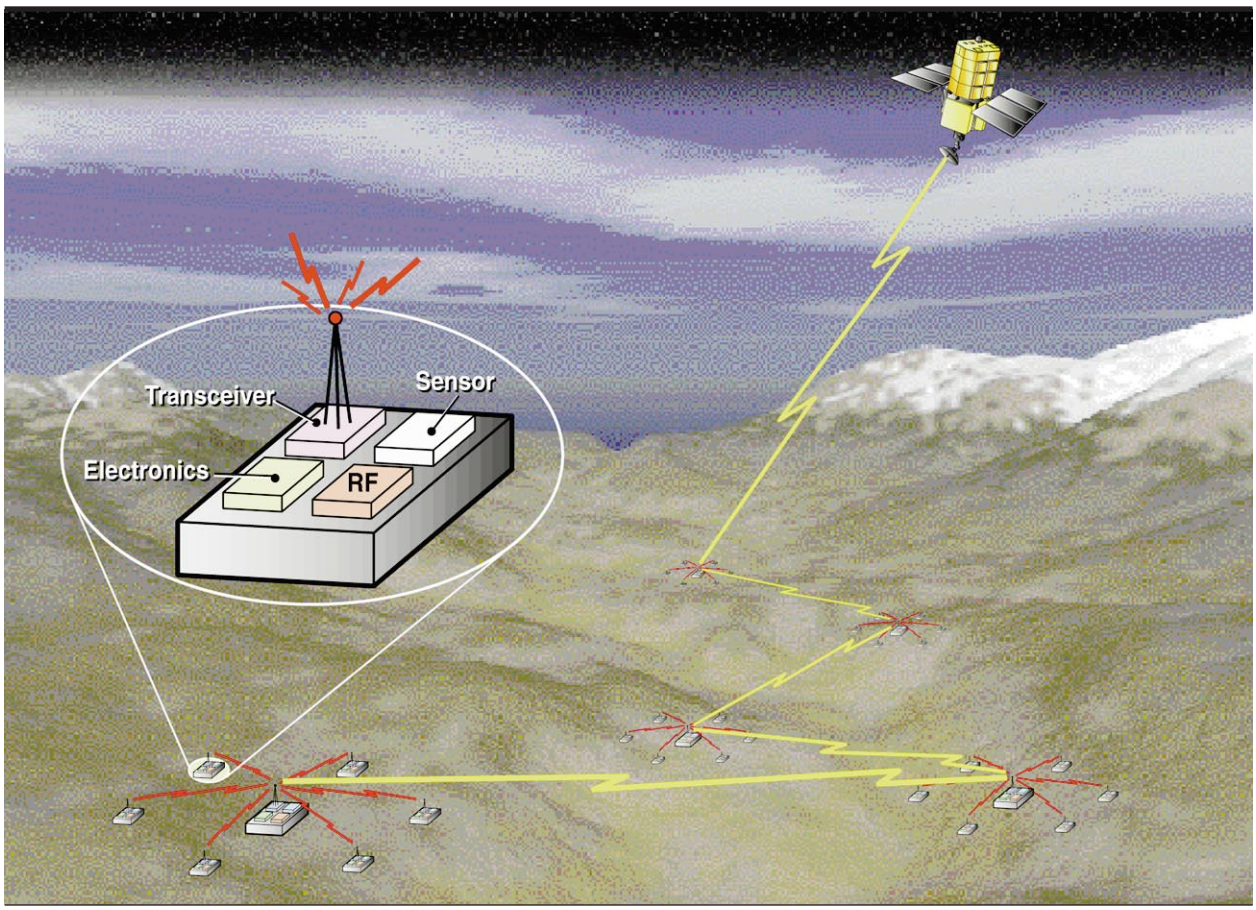

Figure1. Typical network of low power wireless microsensors.

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The focus of our research has been on development of the small low power nodes and less on the overall network topology. However, some consideration of the network must be given when designing the nodes and some consideration of the nodes must be given when designing the network. An individual sensor node contains not only the sensor but also the sensor interface electronics, analog to digital (A/D) converter, logic, RF communication link, antenna, and the battery. Future nodes will also contain some form of signal processing to allow more sophisticated network architectures. The FY98 goal for this project was to make a sensor node with a physical form factor of a 2" x 2" x 2" cube.

Approach

The ultimate approach would be to integrate all the functional pieces onto one monolithic silicon chip. However, there are many dissimilar technologies such as MEMS, RF CMOS, and FPGAS that have to be joined together to form the overall module. With the overall module concept in mind, we chose to use packaging as a way to tie these dissimilar pieces together. This allowed us to leverage existing commercial-off-the-shelf (COTS) parts when applicable and apply the research to the more advanced portions of the module. **Figure 2** shows the module that was built in FY98. The inner structure is shown extended out the top of the case. This structure contains three boards with the top board an RF board, the middle board an RF modem, and the bottom board both the sensor and sensor interface electronics. Two lithium batteries power the module and sit underneath the board stack. The details of both the sensor and RF system will now be presented.

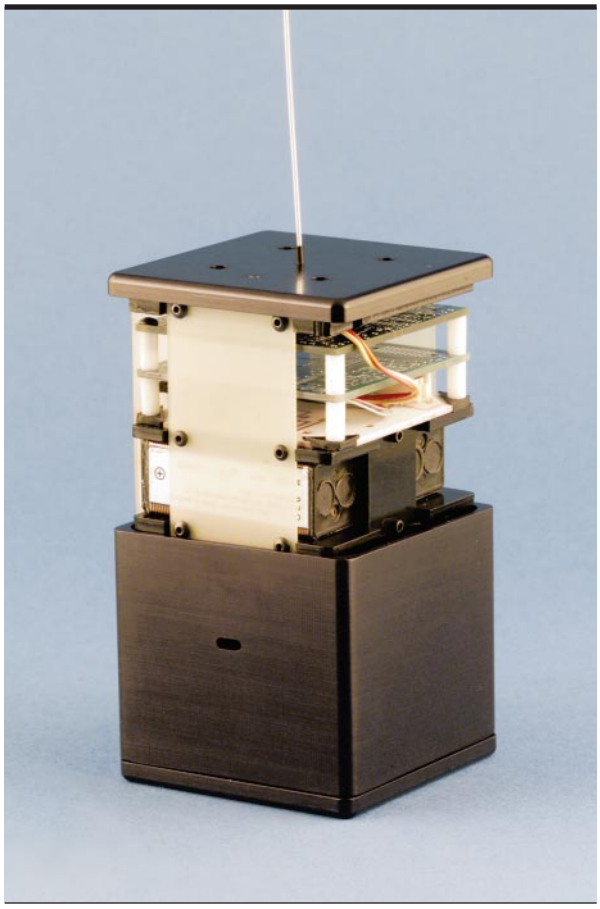

Figure 2. Wireless microsensor module with internal parts shown exposed for clarity.

Sensor

As previously mentioned a variety of sensors might be chosen for any given application. We were directed to look at low µg accelerometers as sensors. These accelerometers can be used to detect ground motion and passing vehicles. Low power and small size were overriding design constraints. Therefore certain types of sensors such as fiber optic devices which require laser power or sensor technologies that require heaters were precluded from our module.

The focus of our work has been on MEMS (Micro Electro Mechanical Sensors) that use capacitive readout electronics. These sensors are almost passive and are both small in size and require minimal power. A MEMS accelerometer uses a silicon proof mass. When a proof mass is accelerated it moves in relation to its surroundings (or package) and the amount of movement is sensed with variable capacitors attached to the proof mass. The effect used to sense acceleration is similar to the crushing feeling felt when one rapidly ascends in an elevator. The sensitivity of accelerometers to low accelerations is inversely proportional to the size of the mass, so we need a relatively large mass to sense µg accelerations (previous work in the literature uses small proof masses fabricated at the surface of the wafer). Our design consists of a thin (2 µm) surface micromachined polysilicon tether which supports a large silicon proof mass carved out of a bulk silicon wafer by deep reactive ion etching (RIE). Deep RIE allows for through wafer etching with aspect ratios of 30:1, thus making these structures possible. A picture of the proof mass after deep etching is shown in **Figure 3**.

In our design the applied acceleration results in the proof mass tilting around the torsional suspension, which magnifies the movement of the mass, resulting in changes in the sense capacitor gaps. A variety of accelerometers were designed with proof

masses ranging in mass from 1.4×10^{-6} Kg to 5×10^{-8} Kg. The resonant frequency of these accelerometers range from a low of 16 Hz to a high of 500 Hz. Lower resonant frequency accelerometers typically have greater sensitivity. In ground sensing application, the lower frequencies tend to propagate the furthest. The design makes use of differential sense capacitors. As the proof mass rotates, one capacitor increases in value while the one at the opposite end decreases in value. The electronics consists of a single ended square pulse drive signal which drives one of the plates on both capacitors. A transimpedance amplifier is attached to the other two plates of these sense capacitors. The currents flowing through both capacitors are subtracted to give a representation of the difference in capacitance between the two capacitive sensors and thus a representation of the movement of the proof mass. Finally, the signal is further amplified and digitized by an A/D converter. The basic sensor requires no power, however, the low power CMOS interface electronics requires a few mw of power.

RF System

The RF system serves to relay the sensor information to a distant monitoring point. The RF system was designed to both transmit and receive. The receive feature at this point is used primarily to poll a particular sensor node. In future network architectures, the receiver becomes more important as nodes will not only communicate with a central point but also with neighbors acting both as sources of data as well as repeater sites for their neighbors.

The transmit RF power level was chosen to be 1mw with an on-the-ground range of about 30 meters. Path loss for RF transmission is proportional to 1 / distance$^{\mathbf{n}}$. For operation close to the ground, **n** can be as high as 4. Typically **n** is closer to 2 for transmission well above the ground. Even with 30 meter propagation, the RF path loss can be as great as 80 dB. RF transmission only occurs on an intermittent basis which reduces electrical power. However, it is important to note that electrical power for a receiver that runs continuously can become the biggest dissipation source. To circumvent this source, a TDMA (Time Division Multiple Access) architecture was chosen to keep the receivers off 90 % of the time. The TDMA scheme helps conserve electrical power but increases complexity at the system level.

The RF transmitter and receiver use direct sequence spread spectrum which gives a low probability of intercept as well as immunity to interference. The chip rate of the spread spectrum modem is 1 MHz and 127 chips / bit gives over 20 dB processing gain with a resultant bit rate of 8 k baud. The spreading and despreading functions are accomplished with a modem which has been implemented in digital logic on an FPGA (Field Programmable Gate Array). The use of the FPGA allowed for easy iteration of the design. The FPGA, in addition to serving as the modem, also provided both logic and memory for buffering data from the sensor and A/D converter.

The modem interfaces with the RF board both on transmit and receive. On transmit, the modem up converts the transmit signals to 916 MHz. On receive, the RF board down converts the 916 MHz signal, digitizes it and feeds it into the modem. A quarter wave wire protrudes from the top of the module and handles both transmit and receive signals.

Technical Accomplishments

- A MEMS accelerometer with µg sensitivity was designed, modeled, and fabricated using both surface and bulk silicon micromachining. Interface electronics for this accelerometer was designed, built and tested. The accelerometer fabrication is being iterated to perfect some of the deep etching steps which are new in our process technology. Fabrication and testing continues on the accelerometer.

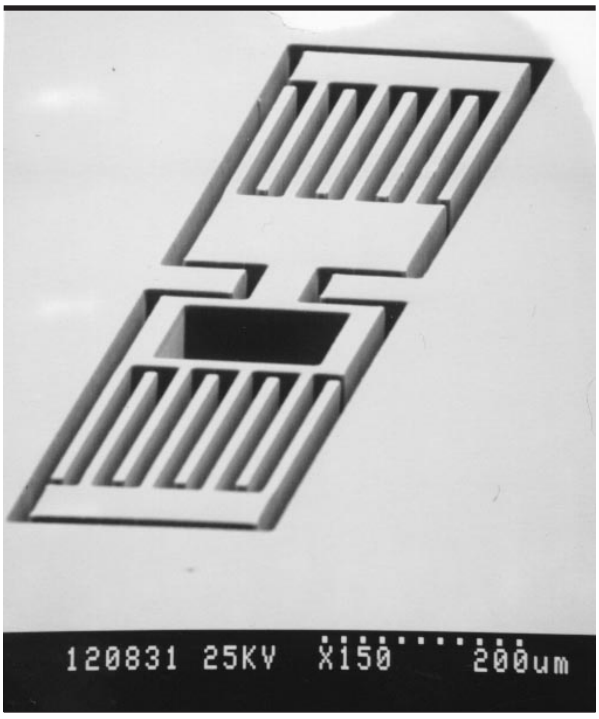

Figure 3. SEM photo of deep etched silicon MEMS accelerometer.

- A spread spectrum RF system was designed, fabricated and tested. The current design occupies two small PC boards with one board containing RF circuitry and the other containing the FPGA which serves as the spread spectrum modem. The modem was specifically tailored to interface with the A/D converter and sensor.
- A compact physical package was designed which houses the sensor, RF system, and batteries. The overall physical package is a cube with inner dimensions of 2" x 2" x 2".
- A TDMA protocol was designed and implemented as a host logic board that interfaces between a PC with a Labview program that acts as a host terminal. The host logic interfaces to a host spread spectrum modem which communicates with the sensor module. The host portion of the project is primarily designed to allow for testing and display of the wireless sensor module data.
- To facilitate the integration of the MEMS sensor with other electronics a flip chip MCM process for packaging was developed, allowing for chip scale packaging of chips from different processes. Packaging of MEMS dies requires special considerations due to the small moving parts found on the die, which makes traditional packaging and encapsulation technologies unfeasible. In addition, MEMS sensors may require contact with a sensing medium, again requiring special packaging considerations.

Summary and Future Plans

Future work will focus on reducing both size and power. These two design specifications are mutually dependent since as power is reduced smaller batteries can be utilized thus reducing overall module size. One of the challenges to achieving low power is reducing receiver current. Newer modem implementations using ASICS should decrease current by a factor of nearly seven. Other RF architectures should lead to power decreases of between fifty and seventy five percent. In the future, we plan to incorporate a commercial signal processor chip within the module. This processor will allow distribution of sensing algorithms among the modules rather than implementation at a central monitor point in a network.